MAX-3D Design Suite

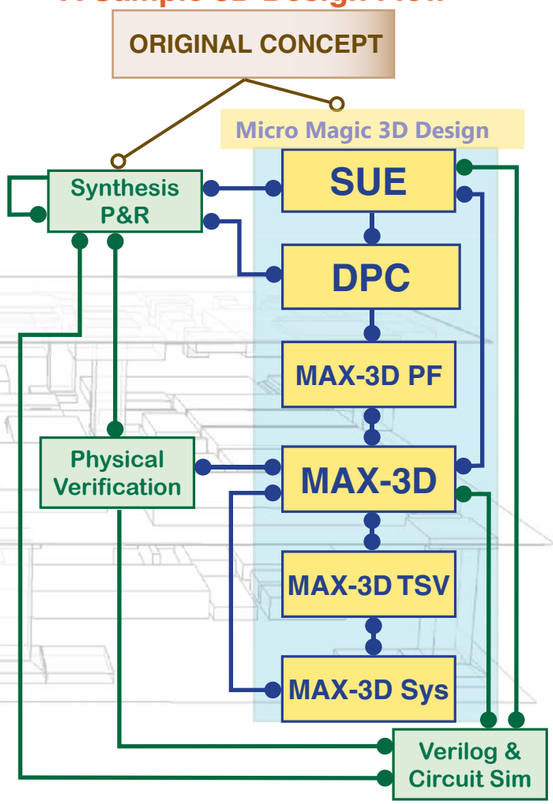
Built on MAX-3D, Micro Magic's native 3D Layout Editor

The MAX-3D-Design Suite contains everything necessary to plan and lay out today's complex wafer-stack and interposer multi-technology designs.

MMI's suite of 3D tools includes DPC-SUE, MAX-3D, MAX-3D TSV Placer, MAX-3D Path Finder

- **Load multiple chips in the same or different technologies.**
- **Manage multiple levels of hierarchy and multiple tech files all at the same time.**
- **Edit and view today's largest designs.**
- **Automatic Connectivity Tracing through multiple levels, even through the package or board.**
- **Show 3D connectivity with fly-lines.**
- **Use your existing 2D Tech files.**
- **View Results in 3D.**

A Sample 3D Design Flow



MAX-3D Design Suite integrates seamlessly with other industry standard tools

DPC-SUE to import designs from either 2D floorplanner or block-level verilog; specify chip level, block size, connectivity; and export floorplan to MAX-3D.

MAX-3D Path Finder, to explore viability of interposer or stacked-die implementations. Do multiple "what-if" studies on many different partitions.

MAX-3D for true 3-dimensional layout, supporting multiple distinct technology files for Through-Si Via 3D wafer-stack and interposer design.

MAX-3D TSV Placer for automatically locating, optimizing and placing TSVs.

MAX-3D System for the first time - your chips, package and PC board all together, in one tool. View, analyze, & edit all of them in one environment. Isolate and extract nets; study signal integrity across all components.

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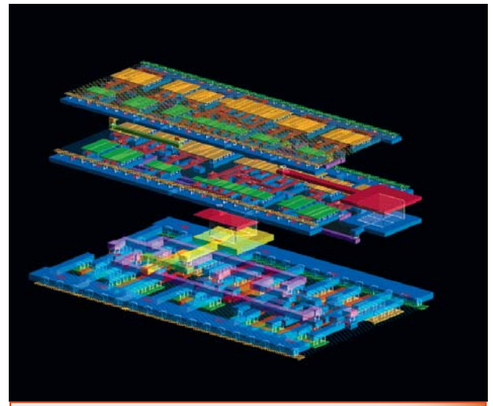
MAX-3D Design Suite

Plan, Build, & Analyze 3D TSV Wafer Stacks

The MAX-3D Design Suite provides everything you need to plan and analyze the benefits of 3D for your design, determine TSV locations, put together 3D wafer stacks, and analyze 3D nets. MAX-3D Design Suite can also be used for 2.5D interposer designs.

- Allows you to quickly do "what if" experiments for analyzing optimal 3D partitioning.
- Automatic TSV placement.
- World's only TRUE 3D design suite.

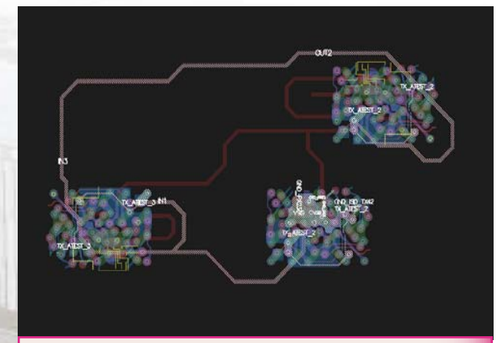


Screenshot of three different wafers & technologies

MAX-3D Design Suite includes **DPC-SUE**, **MAX-3D**, **MAX-3D TSV Placer**, and **MAX-3D Path Finder**.

MAX-3D System for Chip/Package/Board Co-Design

- MAX-3D System is the first software package that allows the user to load, view and analyze chips, packages, and boards all in the same view.
- Allows for chip/package/board co-design and analysis.
- Select & extract nets for analysis.
- Export nets with parasitics and coupling to other tools.



Viewing nets from 3 chips to package to board

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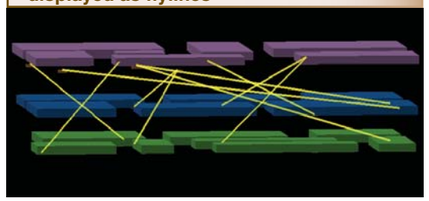
TSV Wafer-Stack Co-Design

MAX-3D TSV Placer

Auto TSV Placement

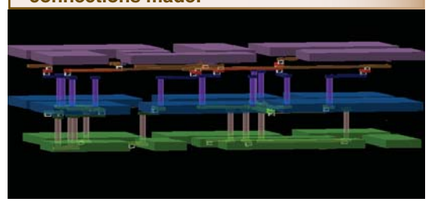
MAX-3D TSV Placer can automatically find legal locations and place TSVs on an entire chip in seconds.

Three stacked die with connectivity displayed as flylines



- Automatically finds "holes" for TSVs.
- Automatically optimizes and places TSVs.

After TSV Placer: TSVs placed and connections made.



- Shows 3D connectivity with fly-lines.
- Exports TSV data back into your 2D tools.

At the beginning of a project, once the 3D floorplan is set, use MAX-3D TSV Placer to determine the best legal locations for TSVs based on connectivity and user-specified "keep out" regions.

MAX-3D TSV Placer can be used in conjunction with MAX-3D Path Finder to improve TSV placement.

If you have existing layout, MAX-3D TSV Placer can help you determine valid locations for TSVs. It also helps figure out and spread apart blocks, if needed, to provide space for valid TSV locations.

MAX-3D TSV Placer can be used at the beginning of a project during floorplanning or toward the end of a project with already designed chips.

MAX-3D System

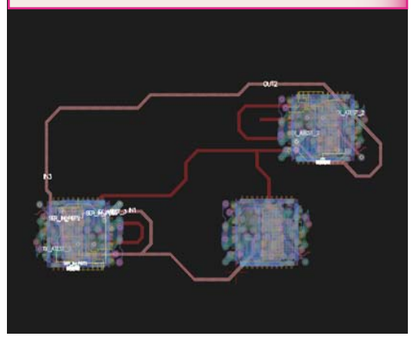
Chip / Package / Board Co-Design

Finally, chip designers and package designers can work together.

MAX-3D System is the first tool capable of loading, analyzing and editing all components from chip to package to board. The chip can be a TSV wafer stack or a single chip.

Using one environment, you can now really visualize and modify the project as an entity, without piecing aspects together from many disparate sources. Unification of the process speeds design efficiency and reduces the potential for error.

Viewing nets from chips to package to board



Extracted net from chip to package

- Chip-to-Board viewing and editing - in 3D.
- Load Chip, Package and Board together, in one tool, and then view, edit and analyze them.
- Isolate and extract nets and study signal integrity from chip, through package, across board, through another package, then to the receiving chip.

MAX-3D Path Finder

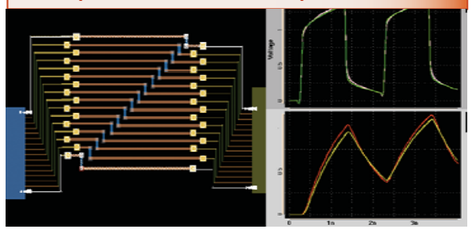
Quick Scenarios for 3D Evaluation

MAX-3D Path Finder is the tool you'll want when evaluating a new proposal:

Will 3D meet our performance needs and power requirements?

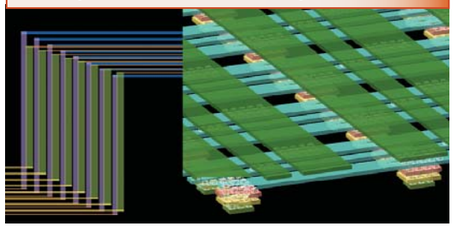
Quickly design and analyze multiple "what if" 3D design scenarios.

Examples of 3D Path Finder capabilities



Two 3D nets selected in 3D design. *Simulation results for two selected nets.*

Examples of 3D Path Finder capabilities



Easily generate complex busses. *Easily generate complex PDN.*

Does 3D work for you? MAX-3D Path Finder can help you answer this question.

- Import Verilog or 2D floorplan.
- Specify/modify 3D floorplan.
- View 3D connections via fly-lines or actual routes.
- Quickly route complex 3D busses to determine delays.
- Extract, analyze and simulate specified 3D nets.
- Automatic PDN (power distribution network) generation for power analysis.

Once you have confirmed the benefit of 3D design, MAX-3D Path Finder will help determine the best partitioning of your design across multiple chips.

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Micro Magic Inc.