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High-End Services Firm Taps I/O

By Gale Morrison

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Sunnyvale, Calif.-based Micro Magic Inc. (MMI) has implemented the final design for a high-performance I/O interface chip for JAZiO Inc. of San Jose. JAZiO is looking to take on Rambus Inc. and dozens of other chip-to-chip communication schemes with this technology, so Micro Magic was happy to get on board.

MMI's last high-profile project was on Malleable Technologies' network processor. The two discussed their collaboration in May and by June PMC-Sierra Inc. had ponied up $231 million to buy the NPU intellectual property.

Mark Santoro, president, Micro Magic Inc.

MMI implemented the JAZiO 2GHz part using its own custom design tools: the SUE design manager, MAX layout editor and DPC datapath compiler.

Collaborating with JAZiO and using their SPICE simulations for the I/O, MMI designed and taped-out the technology demonstration chip in four months. JAZiO has one licensee now and others in the works, according to Bruce Barbara, president and chief executive officer.

The JAZiO I/O technology aims to solve system performance bottlenecks with an approach that employs signal switching in the time domain rather than in the traditional voltage domain. One patent has been issued for the technology and five are pending. It depends on the JAZiO core or chip at both ends of the chip-to-chip communication, one acting as master and one as a slave to communicate the data and then compare it at the receiving end, at very high speeds.

The design MMI completed was the custom physical layout of just 55 transistors per pin; the tricky part was making that design perform at the specified 2GHz that would make it a showstopper.

"This was different from anything we've built," said Mark Santoro, president of MMI. "We looked at their simulations and it looked really good. This I/O is four or five times what Rambus is running at. It's a different and unique idea that no one else has."

Jim Slager, chief evangelist for JAZiO, explained what really brought his company to MMI. "We needed an effective design that's almost as good as custom, but we had to do it very quickly. We said, 'We do need a specialized transistor design,' but we didn't have a lot of time, or a lot of money," Slager said.

"The time and cost of a near-ASIC was what we're looking for," he added. "But for this performance requirement, whenever we talked with any one else (to implement the design) they shied away. Once we started talking 2GHz they said forget it. MMI said, 'Let's do it.' "

MMI did a full custom layout on the actual receiver in the I/O to make it as small as possible. JAZiO is licensed to reuse that layout. JAZiO's licensees can get the design in that format, or a number of others, depending on their needs and where they would be manufacturing.

Santoro said that this type of design does not lend itself to traditional EDA tools.

"This was a design that did not lend itself well to DC (Synopsys' Design Compiler) and place and route (from Avant! or Cadence). You can use a router, but DC is for when you are building more of an ASIC," he said.

"This chip is essentially very high-speed datapaths. The data comes out of this thing in parallel. In that case, the designer needs a tight layout running at very high speed. The designer needs a lot of control over the logic. Our tools give them exacting control over the placement. It's an automated way of building custom datapaths," Santoro said.

The test chip is capable of pattern generation, self-test, internal serial-to-parallel and parallel-to-serial data conversion, programmable internal clock generation (up to 2Gbit/sec. pin-data rate), and data-error collection.