Institute for Microelectronics

Research Activities

Closed-loop Sigma-Delta Sensor Circuits

A variety of detection circuits suited for the measurement of sensors based on micro-mechanical differential capacitors has been thoroughly studied and realized on silicon. In a recent implementation electrostatic force feedback was used in a closed sigma-delta loop for measuring mechanical acceleration. The 4mm2 chip - seen on the right of the sensor - has achieved excellent linearity and extended bandwidth. The hybrid low power micro system provides true 16 bit resolution and a measurement range increased 10-times /1/.

Data Converters

Based on a continuous experience in mixed-signal design, several AD-converters have been developed with special focus on very low power operation at high resolution, but at low data rates. Multi-slope converters have been developed and optimized for a typical 10-year single-battery-operation. Currently we are working on a medium resolution 10 MHz Nyquist-rate AD-converter with extreme constraints on power and silicon area, which will serve, in a future CERN-experiment, in more than a million of simultaneous systems. Very high resolution DA-converters for software radio - based on high order digital sigma-delta - are also under investigation /2/.

Advanced I/O-circuits

Scaling of CMOS-processes requires the reduction of operating voltage to 1 volt or below for a safe operation of the devices. I/O-standards, however, tend to stay at conservative high voltages. This is a demanding conflict for the design of I/O circuitry. We are currently investigating a variety of circuit topologies for I/O-standards like HSTL, LVDS, PCI-X and others. In cooperation with leading semiconductor companies the proprietary cell designs - including new concepts - are implemented on silicon test wafers. Simulation and characterization of ESD-protection devices is covered in a further industry project.

Low Noise Oscillators

Jitter and phase noise of clock oscillators or VCOs is a major concern in fast mixed-signal systems. We have investigated techniques for the transient simulation of low noise oscillators using the so-called "impulse sensitivity function". We are able to evaluate contributions of different noise sources like thermal noise, 1/f-noise, ground bounce etc. on the total noise at each phase of the oscillation cycle. The graphic shows the simulation results of two oscillators that differ significantly in their noise behaviour.

Low Leakage Circuit Techniques for Advanced CMOS

Modern sub-micron processes suffer from substantial high sub-threshold leakage currents due to low threshold voltages. Additionally, decreasing gate oxide thickness enable tunneling currents to flow via the gate. These currents tend to reach the order of drain-source leakage currents. Hence, both effects increase standby power dramatically for complex systems, which is unfavorable especially for handheld devices. New concepts are being investigated that allow to reduce both types of leakage currents, according to the requirements of higher performance and still longer battery life time /3/.

Parameterized Layout Cells for Mixed-Signal System Simulation

Parasitic circuit elements, as calculated from the extraction of the layout view, should be taken into account in a realistic simulation of analog integrated circuits. This, however, requires the repeated and time-consuming layout iteration during the development process. More flexible is the use of parameterized layout modules provided by an analog layout generator. Based on the CAD-Tool MAX-LS ™ of Micro Magic Inc. we have implemented dedicated modules using the graphic script language Tcl/Tk /4/. The layout example on the left is a simple differential amplifier adapting itself to the settings of device and geometry parameters.

References

/1/ C. Lang, R. Tielert: "A Low-Noise Accelerometer with Digital PID-type Controller and Multibit Force Feedback", Proceedings of ESSCIRC 99, Duisburg, Germany, Sept. 1999

/2/ R. Tielert: "D/A-Converters for Broadband Software Radio", Proceedings of Analog Workshop TU Berlin, Berlin, Germany, March 2001

/3/ A. Schmitz, R. Tielert: "A Multi-Threshold Circuit Technique for the 0.13 CMOS Generation", VDE-Fachbericht 162, ITG Workshop, Darmstadt, Germany, Nov. 2000

/4/ U. P pperl, R. Tielert: "Design of Parameterized Layout Cells - a Comparison of suited CAD Tools", Proceedings of Kleinheubacher Tagung, Kleinheubach, Germany, Sept. 2001