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Design Boutique Helps Malleable

By Gale Morrison -- *Electronic News, 5/8/2000*

New York - A little-known network processor start-up and a virtually unknown high-end processor design house that have now come to light make up the true -not forecasted or predicted or theorized-first day of the future of microelectronics.

Mark Santoro,
Micro Magic, Inc.

Malleable Technologies Inc.'s recent **Malleable Embedded Communications Accelerator (MECA)** network processor is one of the largest integrated ICs ever produced (the firm will not say publicly exactly how large). It's a programmable logic- and memory-packed system-on-a-chip (SOC) that came together by purchasing third-party semiconductor intellectual property (IP) and outsourcing millionaire design engineers, and then using an independent billion-dollar foundry, Taiwan Semiconductor Manufacturing Co. (TSMC), to fab it.

Oh, and the design teams did not use synthesis-the nearly indispensable design automation step that turns hardware design language code into structures-for large chunks of the design. And in another portentous shift, the design engineers from Micro Magic Inc., Sunnyvale, Calif., who did this memory compiler work are mostly Ph.Ds who spent nearly all of the 1990s designing microprocessors, not networking ICs.

Telle Whitney, Malleable's vice president of engineering, a bit reluctantly discussed Micro Magic's part in the genesis of MECA, which took place over only the last 12 months. Malleable, based in San Jose, took private and corporate funding last June, said Whitney, though it will not name those investors.

The super-size MECA voice processors are meant for voice over asynchronous transfer mode (VoATM) and voice over Internet Protocol (VoIP) equipment. Each device can process up to 96 channels of compressed voice or 512 channels of uncompressed voice, including ATM or IP packetization. The MECA architecture is said to integrate DSP- and packet- processing functions and replaces more than 10 existing devices, including eight general-purpose DSP chips typically used in current designs. It's known that the transistor count is above 20 million-a space where Pentium IIIs are barely treading. Beyond that, comparisons are tough.

Malleable's Whitney would only say that the Sonics Inc. SiliconBackplane IP was licensed and that Micro Magic completed the design in large part by virtue of the MegaCell memory compiler technology it has. She did not want to discuss whether the design was a DSP array, as many firms are proposing, or how much memory it has on-chip. She said the part is "programmable, but customers won't program it."

"It's a large chip, and it has a lot of memory," she said. "We're trying to stay away from talking about transistor counts. We're shying away from a technology announcement." Whitney and Micro Magic said they did not want competitors to know too much about the design, though it would take those same competitors "months to catch up."

Whitney said the memory in question is embedded SRAM, done by Malleable's foundry TSMC. Micro Magic is now selling a MegaCell compiler that could design such SRAM for $150,000, a comparable price for any other EDA tool on the market. Asked whether the architecture approach is anything like the new league of multi-DSP platforms from Improv Systems Inc., BOPS Inc., or Infinite Technology Corp., Whitney declined comment.

"It's not a chip that Malleable's competitors (who are also the legion of NPU players) are going to have an easy time figuring out," said Mark Santoro, president, chief executive officer, and founder of Micro Magic. "It's very different from those other approaches." Santoro bills MMI as the crème of the crop, where nearly all the designers are Ph.Ds from Stanford, the Massachusetts Institute of Technology, and the like.

Micro Magic for the first time worked the disclosure of its work into a contract, Santoro said. Since the firm's founding in 1995, clients had MMI under nondisclosure, he said. Santoro is now looking to commercialize the specialized datapath generator and layout control EDA tools his designers developed in order to do their high-end work, so the "latest and greatest" splash that Malleable is making should help that.

"The MECA processor is just a really good part for us to go public on," said Santoro. Micro Magic is now seeing a lot of network processor start-ups-though these days more and more are wholly owned subsidiaries-who need this kind of expertise, he added.

"We're seeing a flood of start-ups, now that the VCs (venture capitalists) have found out about us," he said.

The only question now is will MECA work as the intended customers need it to? Cary Ussery, president and CEO of Improv, Beverly, Mass., is not so sure. "In some ways, this is taking general ideas for FPGAs and moving it up a level. My general opinion is that, while the technology looks good on paper for 'pure' algorithms, real-world applications have more complex requirements," Ussery said. "Malleable's technology may work on small algorithmic components, but it won't scale well to full-blown products. I do think this technology can be put together as a possible alternative to the general reconfigurable FPGA approaches being worked out."