Micro Magic Reemerges

Michael Santarini - May 30, 2006

After being purchased for a whopping $260 million by Juniper Networks during the height of the dot-com boom, Micro Magic has reemerged as an independent, privately held, completely bootstrapped design services and EDA company specializing in high-performance digital and mixed-signal design.

Back in 2000, Micro Magic stunned the EDA world when Juniper ponied up $260 million for the 20 or so employee privately owned company. At the time, that was the third highest amount ever paid for an EDA company (behind Cadence's acquisition of Ambit and CCT)—a surprising amount given Micro Magic certainly was not a well known EDA player.

But Mark Santoro, the company's president and CEO then and now, said his company was quietly building very large, fast chips for a select group of companies, most of whom went on to become billion dollar organizations due in large part to Micro Magic's designs.

Santoro takes pride in the fact that the Juniper acquisition afforded every one of his employees the opportunity to "retire if they wanted to."

So, why do it again? Santoro said he was getting bored with early retirement and so he along with a dozen or so of his old employees decided two years ago to make an arrangement with Juniper to spin out the technology. The company, which is has no outside funding has since been reworking and modifying the code for its EDA lineup and is now making it available to the mass market.

The company originally developed the suite out of necessity to fill in the gaps in commercial flows. Santoro said while commercial EDA has caught up in some ways, Micro Magic is still better suited for IC designs requiring bleeding edge performance. The company offers four tools: SUE, MAX, DPC, and MCC.

SUE is the company's front-end tool. It is a large capacity schematic capture tool that also serves as a cockpit for assembling and testing designs. Because a large portion of Micro Magic's work was full custom, the tool needed to have a large capacity and the ability to drill from RT level down to transistors. "You can control what level you netlist things to and tunnel all the way down to transistors and leave everything else as a high level behavioral model," said Santoro.

The tool supports hierarchy and can generate Verilog from a schematic or generate a schematic from Verilog.

SUE can drive Verilog, SPICE or mix of the two simulators. SystemVerilog support is in the works.

On top of SUE, the company offers DPC (DataPath Compiler). DPC takes a graphical image in SUE and generates a placement file in bit slices. It computes a route and then runs static timing from a built-in engine or, if users prefer, Synopsys' PrimeTime. "The tool will then tell you the timing," said

Santoro. "It's really fast and can do 30,000 gates a minute."

Santoro said Micro Magic created the tool for datapath intensive design projects. "We were trying to develop a tool that would give us full custom performance with automation close to an ASIC flow," said Santoro. "The feedback allows you to make logic and architectural changes. It's really hard to tell what's going on when you're looking at a lot of Verilog code going into a black box so what this tool really does is pull out part of that flow that normally takes days going through an ASIC flow and reduces iteration time to minutes allowing you to operate on pieces that are causing time critical problems. You fix it and then insert it back into the flow using a DEF file."

From there, the design can be moved to the company's flagship tool, the MAX layout editor. "MAX looks like just another layout editor but it is fully programmable and it is the fastest layout editor on the planet," said Santoro. "We loaded a customer chip recently that was a 4GByte GDSII file. With all layers on and all hierarchy exposed, it took us about one second to bring it up."

Micro Magic demonstrates a 1 billion transistor design on the system. "The design is not fabable but it demonstrates the speed of the tool," said Santoro.

In addition to speed and capacity, the tool features a large capacity real-time design rule checking. The tool has some built in DRC features but can also run in with Mentor's Calibre.

The fourth tool offering, MCC (MegaCell Compiler), is primarily targeted at folks designing memories, mainly SRAM or ROM, or those designing new FPGA architectures.

"This is for the person actually designing the memories," said Santoro. "It's a programming environment that runs on top of MAX. Unlike old tillers that take a thousand lines of code to program up a thousand word line, it is all algorithmic and understands layout connectivity, so it is a simple loop to do a memory decode. You write a simple loop and it can figure out where all the address and word lines intersect and program them automatically."

Micro Magic isn't seeking venture funding but is looking for more employees. The company's tools start a bit more than $30,000 for an annual subscription.