QUARTERLY TECHNICAL REPORT 1
FOR
Pittsburgh Digital Greenhouse

Electronic Design Technology Development Program
Project Solicitation 00-2

Project Title: HIGH SPEED CMOS ANALOG-TO-DIGITAL CONVERTER
CIRCUIT FOR RADIO FREQUENCY SIGNAL

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Report Period: 12/1/2000 to 4/2/2001

URL for this report: http://www.cse.psu.edu/~chip/pdg/rp1/report1.html
Report Slides(.ppt): http://www.cse.psu.edu/~chip/pdg/rp1/report1.ppt

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1. Summary of the Quarterly Technical Report 1

Click here for the report summary in PDF format.

PROJECT GOALS FOR THIS QUARTER

(1) Design a 6 and 8 bit TIQ based flash ADC circuits and CMOS layout
(2) Design the first prototype chip: 6 and 8 bit flash ADC
(3) Chip fabrication submission

ACCOMPLISHED PROJECT MILESTONES FOR THIS QUARTER

(1) Designed a 6, 8, and 9 bit TIQ based flash ADC circuits and CMOS layout in 0.25 um technology
   a. Total six ADCs are designed:
      i. a 6bit high speed ADC
      ii. a 6bit low power ADC
      iii. an 8bit high speed ADC
      iv. an 8bit low power ADC
      v. a 9bit high speed ADC
      vi. a 9bit low power ADC
   b. Circuit design, layout design, simulation, verification, and synthesis
   c. TIQ comparator section design and thermometer code-to-binary code encoder design
   d. TIQ comparator layout generator program design
   e. ADC power optimization

(2) Designed the first prototype chip: 6, 8, and 9 bit flash ADC

a. Custom pad-frame design
b. Floor-plan design and place \& route 6, 8, and 9 bit ADCs (total six ADCs)
c. Chip design simulation, verification, and synthesis

(3) Fabrication submission preparation

(4) Chip fabrication submission
a. Submission date: 4/2/2001
b. Vendor: MOSIS with TSMC 0.25 um foundry
c. Expected prototype chip delivery date: 7/16/2001

FACULTY AND STUDENTS SUPPORTED

(1) Principal Investigator: Kyusun Choi, Assistant Professor, Department of Computer Science and Engineering
(2) Graduate Assistant 1: Jincheol Yoo, Ph.D. student, Department of Computer Science and Engineering
(3) Graduate Assistant 2: Daegyu Lee, MS student, Department of Computer Science and Engineering

PUBLICATION

Paper Accepted (during this quarter) to Appear: J. Yoo, K. Choi, and A. Tangel, *A 1-GSPS CMOS Flash Analog-to-Digital Converter for System-on-Chip Applications*, the IEEE Computer Society Workshop on VLSI.

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2. Design Method

1. Systematic Variation Approach

The thresholding inverters are the key to the TIQ based ADC circuit. For an n-bit ADC, total (2**n)-1

TIQ comparators are required. Each of the (2**n)-1 TIQ comparators are different from each other. We use special layout technique to generate (2**n)-1 unique comparators, the Systematic Parameter Variation (SPV) technique. The SPV technique is based on the spice parameter provided by the chip fabrication vendor. The comparator generation steps are as follows:

1. Decide on ADC input voltage operating range
2. Decide on ADC precision n : 6, 8, or 9 bit
3. Determine the ADC quantization step voltage: Divide the ADC input voltage operating range by (2**n)-1
4. Determine the (2**n)-1 ADC quantization voltage
5. Decide the MOS transistor length parameter, L. With smaller L, faster ADC is obtained; however, with smaller L, the resulting ADC consumes more power.
6. Determine the MOS transistor width parameter W through spice simulation. Determine the maximum W for NMOS transistor (Wn) and maximum W for PMOS transistor (Wp).
7. Systematically vary Wn and Wp, generate inverters, simulate inverters with spice, and determine inverter threshold voltages.
8. Among the inverter threshold voltages, find the matching voltages for the (2**n)-1 ADC quantization voltages.
9. Collect and array the (2**n)-1 inverters with matching threshold voltages.
10. Build (2**n)-1 TIQ comparators, each comparator consists of two inverters of the same parameters, connected in cascade.

2. CAD Tool

The set of commercial CAD tools used are:

1. MAX layout editor by Micro Magic Inc.
2. SUE schematic capture tool by Micro Magic Inc.
3. Hspice circuit simulation tool by Avanti Inc.

The optimal design of TIQ based ADC requires many iteration of the SPV technique outlined above. We custom designed a set of C programs to quickly iterate the SPV technique.

1. mkinv.c
2. fndsizes.c
3. buildcomp.c

The listings of these programs are included in Appendix A.

3. Experiment base, Spice Model Base

Our chip fabrication vendor is MOSIS, we used MOSIS supplied 0.25um TSMC CMOS spice parameters. The particular spice parameters we used are proprietry information and they are not included in this report. The sample MOSIS spice parameters (similar to what we used) that are open to public can be accessed at MOSIS web page under Technical Support.

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3. Chip Layout Design

(1) Designed a 6, 8, and 9 bit TIQ based flash ADC circuits and CMOS layout in 0.25 um technology

a. Total six ADCs are designed:
   i. a 6bit high speed ADC
   ii. a 6bit low power ADC
   iii. an 8bit high speed ADC
   iv. an 8bit low power ADC
   v. a 9bit high speed ADC
   vi. a 9bit low power ADC
b. Circuit design, layout design, simulation, verification, and synthesis
c. TIQ comparator section design and thermometer code-to-binary code encoder design
d. TIQ comparator layout generator program design
e. ADC power optimization

- Dimmensions & Layouts

ADCs	Size(W*H) um	Area(mm^2)	Layout
6bit (0.24um) +	198.740 * 256.350	0.051	click
6bit (1.00um) *	289.480 * 352.350	0.102	click
8bit (0.24um) +	301.410 * 841.650	0.254	click
8bit (0.50um) *	331.560 * 969.650	0.322	click
9bit (0.50um) +	339.720 * 1868.550	0.635	click
9bit (1.00um) *	512.250 * 1612.550	0.826	click

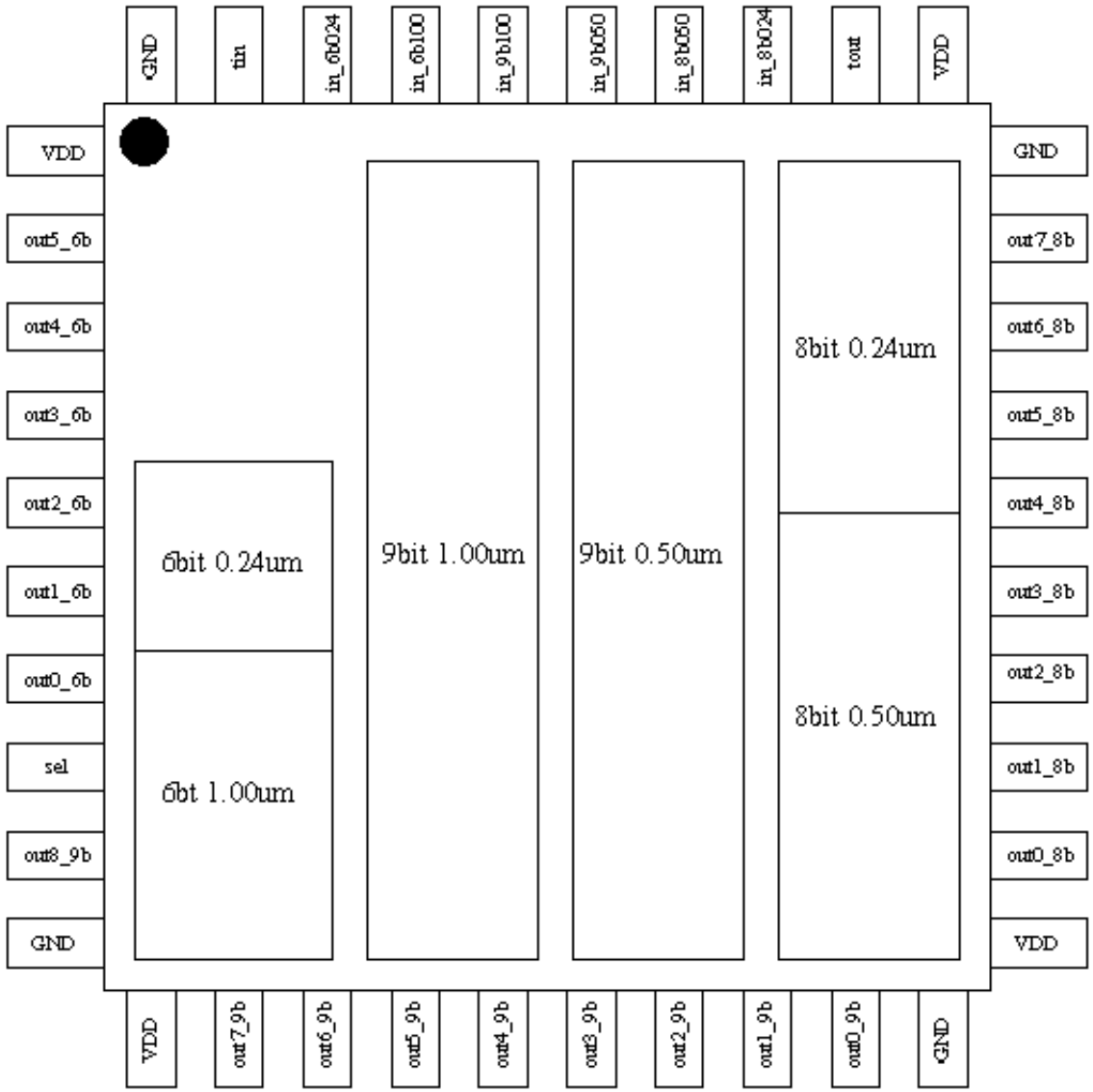
(+: For High Speed, *: For Low Power)

(2) Designed the first prototype chip: 6, 8, and 9 bit flash ADC
  a. Custom pad-frame design
  b. Floor-plan design and place \& route 6, 8, and 9 bit ADCs (total six ADCs)

- Pad
  Size(W*H): 2580 um * 2580 um
  Layout

- Multiplexor
  Size(W*H): 15.450 um * 14.530 um
  Layout

- Chip Block Diagram


GND
tin
in_6b024
in_6b100
in_9b100
in_9b050
in_8b050
in_8b024
tout
VDD
VDD
out5_6b
out4_6b
out3_6b
out2_6b
out1_6b
out0_6b
sel
out8_9b
GND
GND
out7_8b
out6_8b
out5_8b
out4_8b
out3_8b
out2_8b
out1_8b
out0_8b
VDD
6bit 0.24um
6bt 1.00um
9bit 1.00um
9bit 0.50um
8bit 0.24um
8bit 0.50um
VDD
out7_9b
out6_9b
out5_9b
out4_9b
out3_9b
out2_9b
out1_9b
out0_9b
GND

- Chip Layout

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4. Simulation Results

Chip design simulation, verification, and synthesis

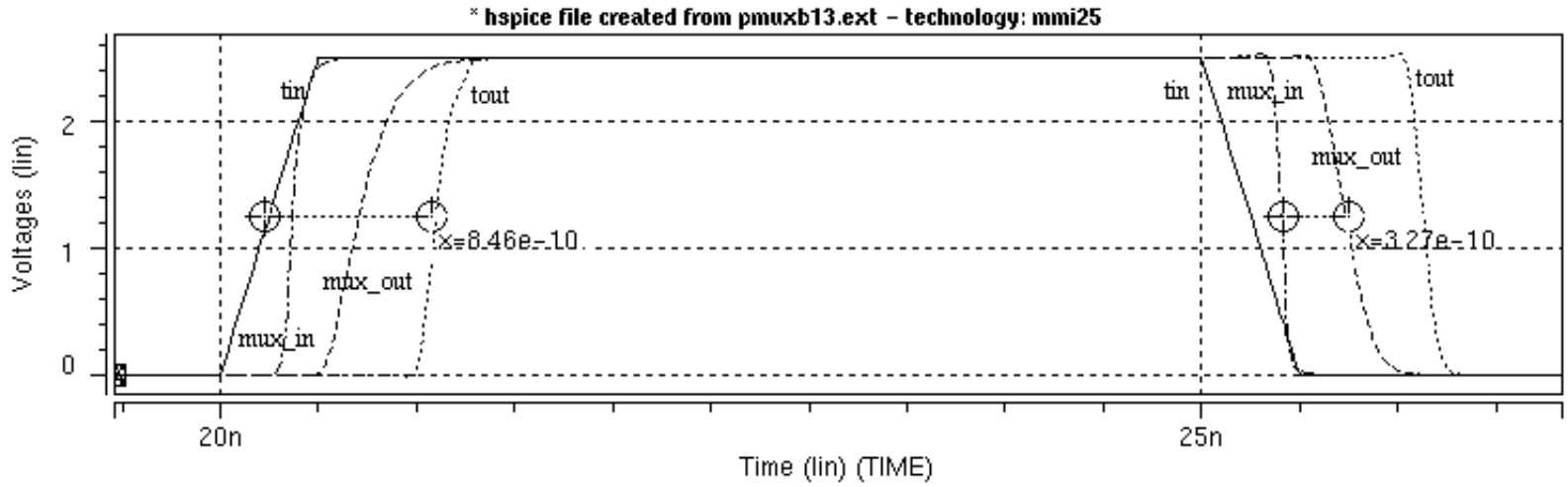
- Speed & Power Consumption

ADCs	Max. Speed (MSPS)	Max. Current (mA)	Avg. Power (mW)	Max. Power (mW)	Result
6bit (0.24um) +	1000	41.80	68.98	102.76	click
6bit (1.00um) *	400	29.36	37.57	70.03	click
8bit (0.24um) +	667	139.08	254.76	353.78	click
8bit (0.50um) *	500	99.34	165.29	254.87	click
9bit (0.50um) +	250	166.79	317.40	469.46	click
9bit (1.00um) *	200	145.38	260.11	417.15	click

(+: For High Speed, *: For Low Power)

- INL, DNL: to be done in the next report
- Sampled sine wave spectrum: to be done in the next report
- Process variation: WVLSI paper
- Pad & Multiplexor

- 'tin' to 'tout' Delay (Minimum Signal Delay): 8.64e-10 sec.
- Muliplexsor Delay: 3.32e-10sec.



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5. Fabrication Submission

(1) Fabrication submission preparation

(2) Chip fabrication submission

a. Submission date: 4/2/2001
b. Vendor: MOSIS with TSMC 0.25 um foundry
c. Expected prototype chip delivery date: 7/16/2001
d. GDSII file (45MB, use "Save as" to download the file)

(3) Project Status:

a. Design number 62265 status is QUEUED FOR FAB
b. Design name is "chip4"
c. Technology is TSMC25.
d. Fabrication restricted to TSMC only.
e. This project can be fabricated on a TSMC_025SPPM run.
f. Layout format is GDS COMPRESSED.
g. Top or root structure is "chip4".

h. Layout file is complete; Binary CRC checksum is 2144600049, 134471442
i. Counted 40 bonding pads.
j. The layout size is 2580 x 2580 microns.
k. Layers found: CONTACT, METAL1, METAL2, METAL3, METAL4, METAL5, N_PLUS_SELECT, N_WELL, PASSIVATION, POLY, P_PLUS_SELECT, RPO, THIN_OXIDE, VIA, VIA2, VIA3, VIA4, VTD_N
l. Requested package is DIP40
m. Requested quantity is 25 (0 unpackaged)
n. You ordered a total of 25 parts
o. 25 to be packaged in DIP40
p. The charge for project fabrication will be $11350.00

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6. Evaluation/Future Work/Conclusion

(1) Features of the TIQ based ADC:
a. High-speed
b. Relatively small area
c. Relatively low-power

(2) Issues to be addressed in future:
a. Dynamic fine-tuning
b. Supply voltage variation compensation
c. Temperature variation compensation
d. Process variation compensation
e. Lower power
f. FIFO design for on-chip high-speed data acquisition

Appendix

(1) Program sources
mkinv.c; making inverters of specified range of size
fndsizes.c; finding desirable sizes of inverter
buildcomp.c; building up a comparator part using selected inverter sizes in previous step.

(2) Presentation slides
Click here for the presentation slides (Power Point file).

(3) Schematics of 3bit TIQ based ADC
Click here for the schematics
